

Project 05 - incremental development

C Coding

Data Representation → IEEE 754
Memory FP

RISC-V Assembly

RISC-V Machine Code

RISC-V Emulator

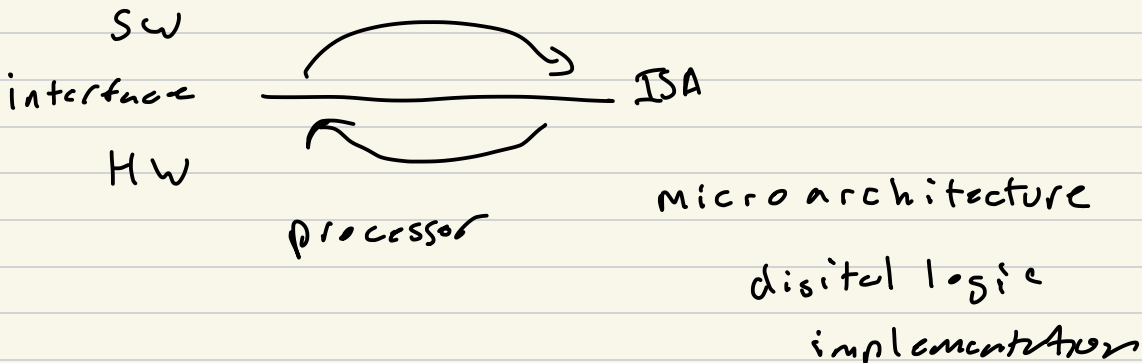
Cache Design

Digital Design



Processor Design

Instruction Set Architecture



Computer Architecture

Instruction Set
Architecture
specification

micro architecture

machine code registers
memory

assemblers
compilers

Digital Design

Schematic
entry
(visual)

HDL
Hardware
Description
Language

Mooce's Law

The number of transistors
in a processor will double
every 1.5 years.

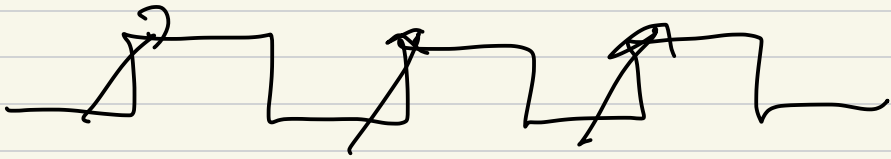
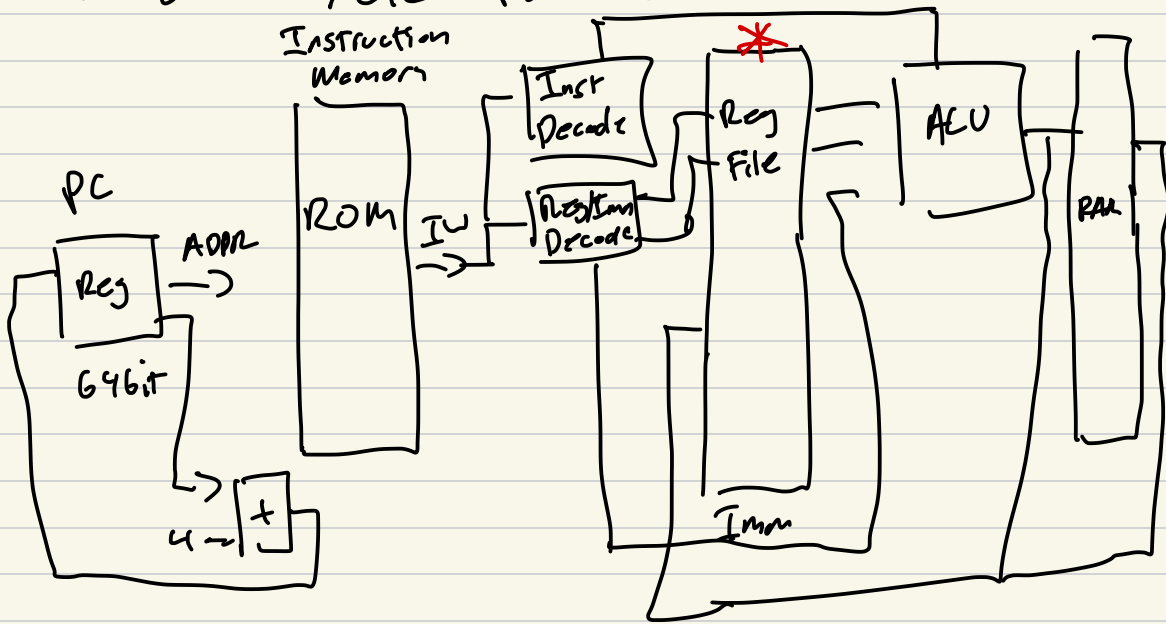
Verilog

IEEE
VHDL

- * single-cycle processor
- * multi-cycle processor
- * pipelined processor

Lab 07 → Lab 10 →
project 06

Single-Cycle Processor



Register File

- 32 64-bit registers: $x_0, x_1, \dots, x_{31}$
- Read up to two registers in the same clock cycle
- Write to one register in a clock cycle.
- x_0 (zero) is always zero(0).



RR read register

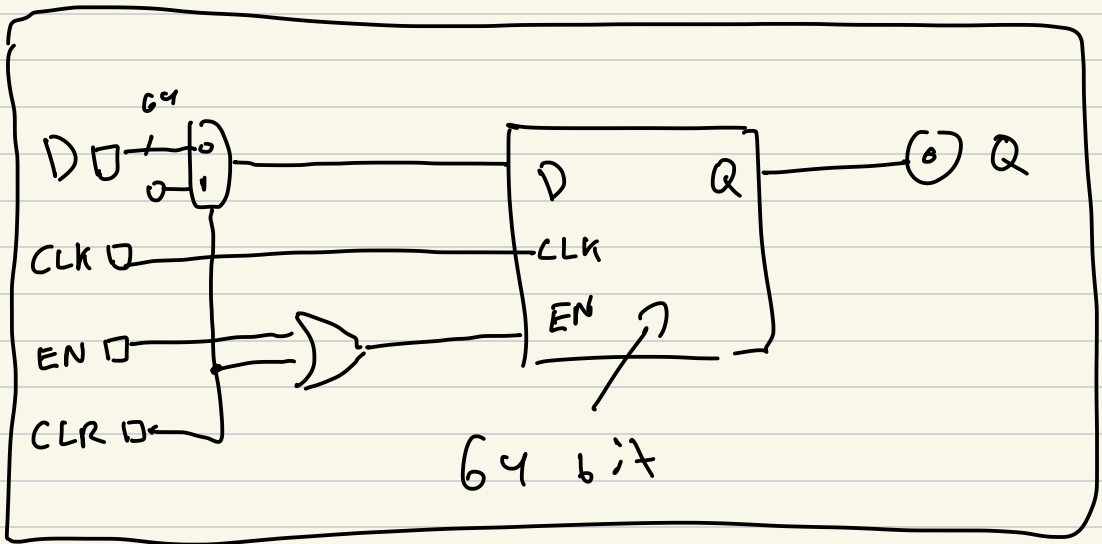
WR write register

RD read data

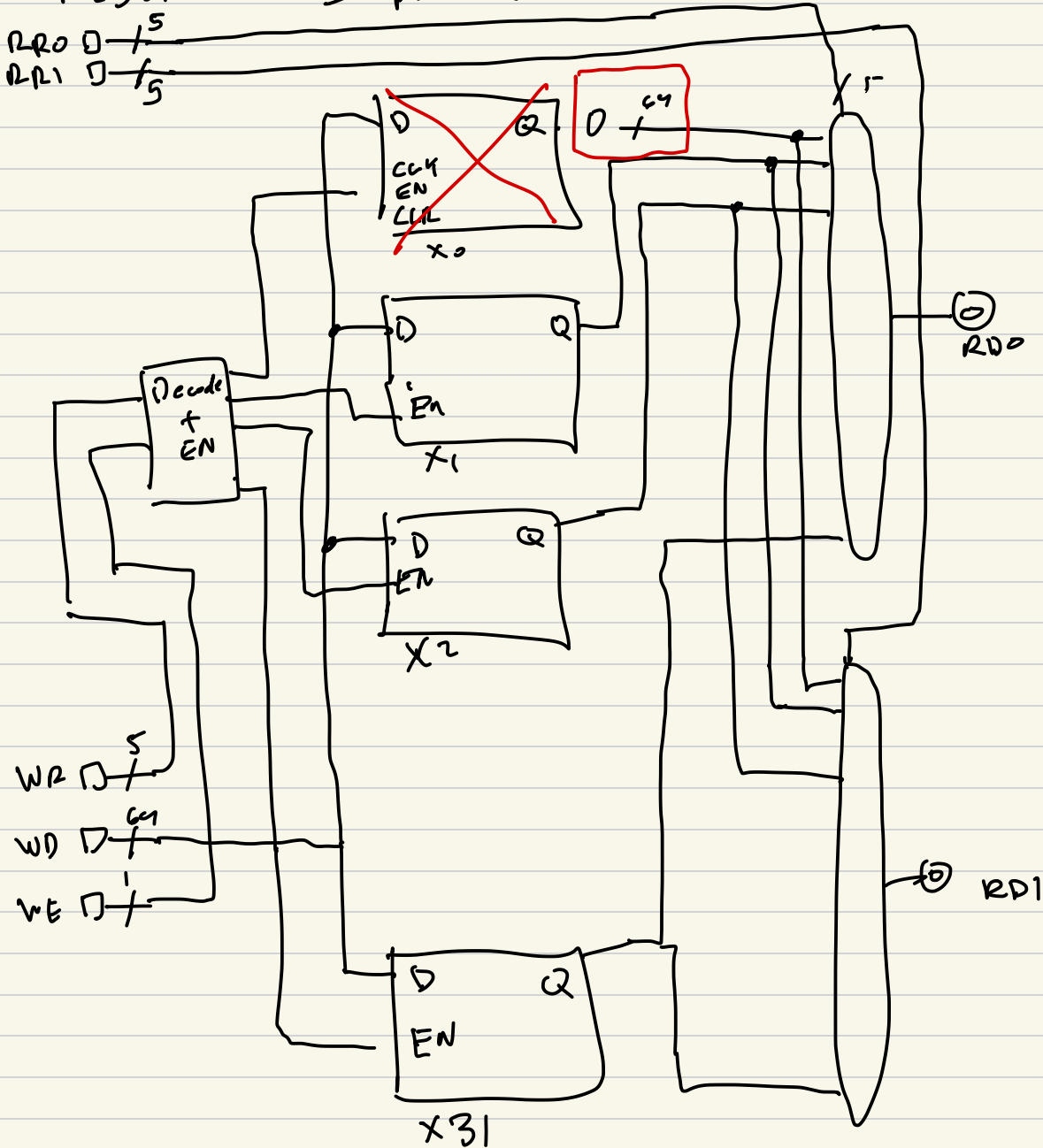
WD write data

WE write enable

Adding CLR to the Digital Register



Register File Implementation



ALU Arithmetic Logic Unit

